

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Withdrawn): A semiconductor device comprising:

a semiconductor circuit which is formed inside of said semiconductor device;

an electrode structure which is formed on a first surface of the semiconductor device;

and

a protective film which is formed of PI (polyimide resin) on said first surface,

said electrode structure including a first electrode layer and a metal plating layer, said

first electrode layer being formed of AL (aluminum) so as to have a thickness equal to or

more than 0.5 μm and connected to said semiconductor circuit, said metal plating layer being

formed of a second metal on said first electrode layer by a wet electroless plating, and said

second metal including at least one of Ni (nickel) and Cu (Copper);

wherein said metal plating layer is selectively formed in a region of said first electrode layer using said protective film as a mask, and

said second metal is capable of being soldered onto an extraction electrode outside of said semiconductor device.

Claim 2 (Withdrawn): A semiconductor device according to claim 1,

wherein said semiconductor device is a MOS high power semiconductor device which further comprises a second electrode layer which is formed of a third metal on a second surface which is the opposite surface to said first surface,

said first electrode layer forms at least one of a gate electrode and a source electrode,

and

said second electrode layer forms a drain electrode.

Claim 3-8 (Canceled).

Claim 9 (Currently Amended): A package for semiconductor device comprising:
a semiconductor ~~device~~ chip including a semiconductor circuit and an electrode structure, said semiconductor circuit being formed inside of said semiconductor ~~device~~ chip, said electrode structure being formed on a first surface of said semiconductor ~~device~~ chip and having a first electrode layer and a metal plating layer which is formed on said first electrode layer,

said first electrode layer being formed of a first metal and connected to said semiconductor circuit,

said metal plating layer being formed of a second metal, said second metal being capable of being soldered onto an extraction electrode outside of said semiconductor ~~device~~ chip;

a supporting substrate which supports thereon said semiconductor ~~device~~ chip;
a lead terminal which is ~~formed of a third metal and~~ electrically connected to said first electrode layer; and

a metal plate which is formed of a ~~fourth~~ third metal to serve as said extraction electrode and which connects said lead terminal to said first electrode layer via said metal plating layer.

Claim 10 (Currently Amended): A package for semiconductor device according to claim 9, which further comprises a protective film which is formed on said first surface, wherein said metal plating layer is selectively formed in a region of said first electrode layer by using said protective film as a mask.

Claim 11 (Currently Amended): A ~~package for~~ semiconductor device according to claim 9, wherein said first metal is AL (aluminum), and said first electrode layer has a thickness of 0.5 μm or more.

Claim 12 (Currently Amended): A ~~package for~~ semiconductor device according to claim 9, wherein said metal plating layer is formed by a wet electroless plating.

Claim 13 (Original): A ~~package for~~ semiconductor device according to claim 9, wherein said second metal includes at least one of Ni (nickel) and Cu (copper).

Claim 14 (Currently Amended): A ~~package for~~ semiconductor device according to claim 10, wherein said protective film is formed of PI (polyimide resin).

Claim 15 (Currently Amended): A ~~package for~~ semiconductor device comprising:
a MOS high power semiconductor ~~device~~ chip including a semiconductor circuit and an electrode structure, said semiconductor circuit being formed inside of said semiconductor ~~device~~ chip, said electrode structure being formed on a first surface of said semiconductor ~~device~~ chip and having a first electrode layer, a metal plating layer and a second electrode layer,

 said first electrode layer being formed of a first metal and connected to said semiconductor circuit, said metal plating layer being formed of a second metal on said first electrode layer, said second electrode layer ~~being formed of a third metal~~ formed on a second surface which is the opposite surface to said first surface, said second metal being capable of being soldered onto an extraction electrode outside of said semiconductor ~~device~~ chip, said

first electrode layer and said metal plating layer forming at least one of a gate electrode and a source electrode and said second electrode layer forming a drain electrode;

a frame plate which is formed of a fourth metal, supports said semiconductor device chip on said second surface of said semiconductor device chip and is connected to said second electrode layer;

a lead terminal which is formed of a fifth metal and is electrically connected to said first electrode layer; and

a metal plate which is formed of a sixth third metal to serve as said extraction electrode and which connects said lead terminal to said first electrode layer via said metal plating layer.

Claim 16 (Currently Amended): A package for semiconductor device according to claim 15, which further comprises a protective film which is formed on said first surface, wherein said metal plating layer is selectively formed on in a region of said first electrode layer by using said protective film as a mask.

Claim 17 (Original): A package for semiconductor device according to claim 15, wherein said first metal is AL (aluminum), and said first electrode layer has a thickness of 0.5 μm or more.

Claim 18 (Original): A package for semiconductor device according to claim 15, wherein said metal plating layer is formed by a wet electroless plating.

Claim 19 (Original): A package for semiconductor device according to claim 15, wherein said second metal includes at least one of Ni (nickel) and Cu (copper).

Claim 20 (Original): A ~~package for~~ semiconductor device according to claim 16, wherein said protective film is formed of PI (polyimide resin).

Claim 21 (Currently Amended): A ~~package for~~ semiconductor device according to claim 9,

wherein said semiconductor device chip is a MOS type high power semiconductor ~~devicee chip~~ which further comprises a second electrode layer which is formed ~~of a third metal~~ on a second surface which is the opposite surface to said first surface,

said first electrode layer forms at least one of a gate electrode and a source electrode, and

said second electrode layer forms a drain electrode.

Claim 22 (New): A semiconductor device according to claim 9, which further comprises a protective film formed of PI (polyimide resin) on said first surface, and

wherein said electrode structure includes a first electrode layer and a metal plating layer, said first electrode layer being formed of Al (aluminum) so as to have a thickness equal to or more than 0.5 μm and connected to said semiconductor circuit, said metal plating layer being formed of a second metal on said first electrode layer by a wet electroless plating, and said second metal including at least one of Ni (nickel) or Cu (copper);

said metal plating layer is selectively formed in a region of said first electrode layer using said protective film as a mask, and

said second metal is capable of being soldered onto an extraction electrode outside of said semiconductor chip.

Claim 23 (New): A semiconductor device according to claim 15, which further comprises a protective film formed of PI (polyimide resin) on said first surface, and wherein said electrode structure includes a first electrode layer and a metal plating layer, said first electrode layer being formed of Al (aluminum) so as to have a thickness equal to or more than 0.5 μm and connected to said semiconductor circuit, said metal plating layer being formed of a second metal on said first electrode layer by a wet electroless plating, and said second metal including at least one of Ni (nickel) or (Cu) copper; said metal plating layer is selectively formed in a region of said first electrode layer using said protective film as a mask, and said second metal is capable of being soldered onto an extraction electrode outside of said semiconductor chip.